Digital Design Systems

Pant 2   Logic Design   pant 1   VHDL

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AND

F

↓   if all input = 1

$F = A \cdot B \cdot C \cdots$

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

2^n

OR

$F = A + B + C$

↓   if any input = 1

Inverter (NOT)

A	$\bar{A}$
0	1
1	0

NAND

NOR

XOR
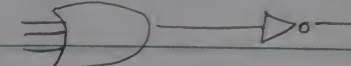
$\frac{1}{}$ if no. 1 input odd

X	y	F
0	0	0
0	1	1
1	0	1
1	1	0

$F = x \oplus y$

XNOR

$\frac{1}{}$ if no. 1 input even

X	y	F
0	0	1
0	1	0
1	0	0
1	1	1

$F = x \odot y$

Kernap map

$$F' = AC + A'C'$$

$$F = (A' + C')(A + C)$$

product of sum

product of max term (مضروب)

$$F = A'C + AC'$$

Sum of product

Sum of min term (مجموع)
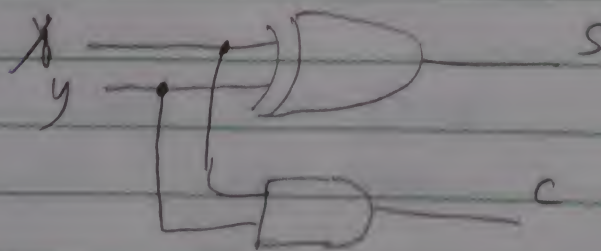
$$F = C' + \bar{A}\bar{B} + \bar{A}\bar{D}$$

Adder

Half Adder

X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$S = X \oplus Y$$

$$C = XY$$

Full Adder

X	y	z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1
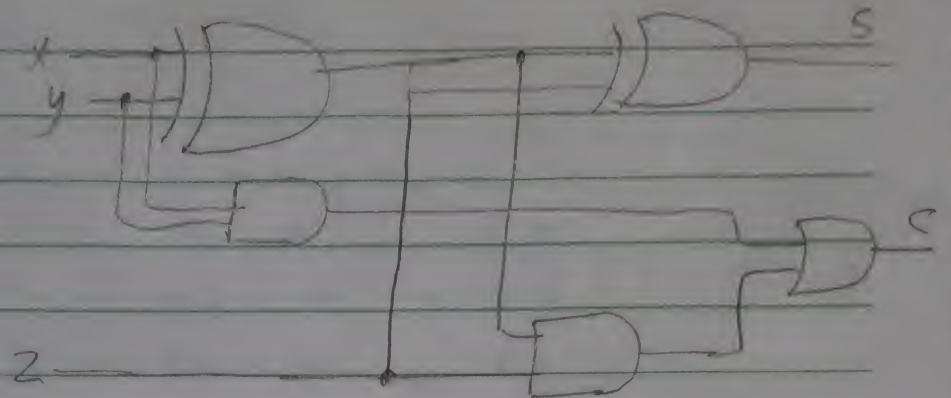
$S = X \oplus y \oplus z$

$C = (X \oplus y) \cdot Z + Xy$
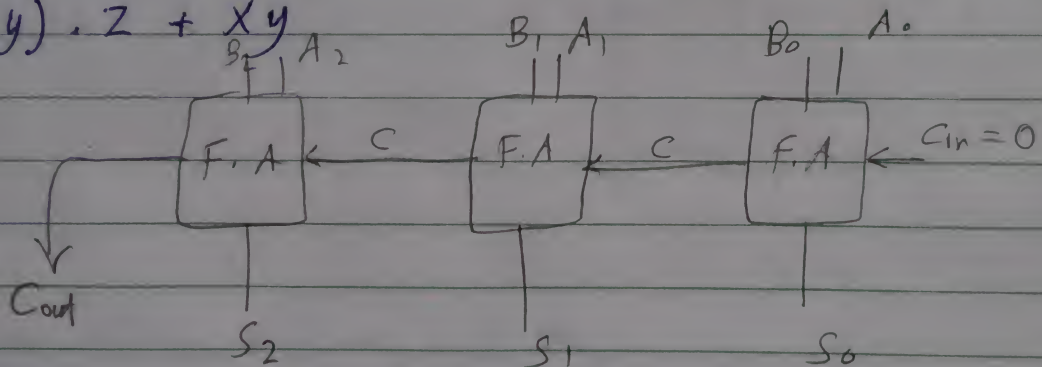
$$\text{Carry Delay} = 2n + 2 \quad \text{gate delay}$$

Carry look Ahead

$$\text{Carry Delay} = 4 \quad \text{gate delay}$$

Decoder

n inputs 2^n output

X	y	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

$D_0 = m_0 = x'y'$

$D_1 = m_1 = x'y$

$D_2 = m_2 = xy'$

$D_3 = m_3 = xy$
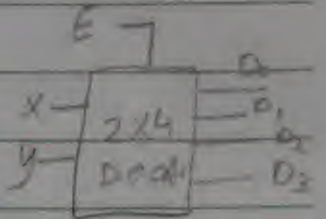
High E   on E = 1

Low E   on E = 0

multiplexer   Mux

S_1	S_0	Z
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Input (2^n)

Select

$$Z = I_0 m_0 + I_1 m_1 + I_2 m_2 + I_3 m_3$$